WELCOME TO ESSDERC 2010

GENERAL CHAIRS'S MESSAGE

On behalf of the Organizing Committees of ESSDERC 2010, it is our pleasure to welcome you to the 40th European Solid-State Device Research Conference. ESSDERC 2010 runs parallel to his sister conference ESSCIRC 2010, covering all aspects of modern solid-state systems, circuits and devices at a single event. In combination, these two conferences provide a unique forum where technologists, device experts, and circuit and system designers can interact. This interaction is instrumental to fully exploiting the potential of modern devices and technologies when confronting the challenges of system-on-chip (SoC) integration. As a delegate at ESSDERC-ESSCIRC 2010 you will have the opportunity to learn of the latest advances in these fields, and to meet those who have dared, pioneered, and succeeded.

The conferences are to be held at the Barceló Hotel Renacimiento, on the Isla de la Cartuja, an island located between two branches of the Guadalquivir river which today is home to the Cartuja 93 technology business park. Seville's downtown (El Centro) is very close by and, from there, visitors will find Seville's major monuments and shops just a few short steps away.

This year, a total of 193 submissions originating from 29 countries were received for ESSDERC including 129 papers coming from Europe, 39 from Asia-Pacific, 15 from North America and 10 from the Middle East and Africa. This is proof of the truly international nature of ESSDERC. The Technical Program Committee with about 110 world-class experts from academia and industry selected 95 papers for oral presentation. Twelve plenary presentations by guest speakers complete the program by focusing on highly relevant topics selected by the Technical Program Committees of both conferences. In addition to the conference programs, a pre-conference day with introductory tutorials and a post-conference day with workshops showcasing work currently being carried out by European research consortia will also be held.

We would like to thank the Steering Committee of ESSDERC-ESSCIRC for giving us the opportunity to organize this event.

WELCOME TO ESSDERC 2010

GENERAL CHAIRS'S MESSAGE

The meeting has been organized by members of the Institute of Microelectronics of Seville (CNM-CSIC), the University of Seville and the University of Granada. We would like to thank the authorities of these institutions for allowing us to devote part of our time to the organization.

We have been extremely fortunate to have the help of an outstanding team of volunteers of the Organizing Committee and the Technical Program Committee, who have all worked very hard. We are hugely indebted to all these volunteers. Our warm thanks to all of them for their dedication, enthusiasm and professionalism.

Last but not least, we would like also to express our greatest appreciation to all the authors who submitted papers to the conference and to all delegates, tutorial lecturers and plenary speakers who have travelled to Seville to interact and share their thoughts during the Conference. They will play a leading role at the event.

Enjoy ESSDERC-ESSCIRC 2010 and your visit to Seville. We hope to see you all back here more often!

Welcome / Bienvenidos!!

José L. Huertas
Ángel Rodríguez-Vázquez
General Chairs - ESSDERC-ESSCIRC 2010

ABOUT UNIV. OF GRANADA

The Universidad de Granada, founded in 1531, continues a long teaching tradition, the roots of which can be traced back to the madrasahs of the last Nasrid Kingdom.

The University is a vibrant presence in the city of Granada, benefiting from the distinctive beauty of its environment and a privileged geographical location due to its proximity to the Sierra Nevada, an excellent ski resort and the Mediterranean coast, with several major tourist sites, including Motril, Almuñécar and Salobreña.

In Granada, there are four University Campuses, as well as the "Campus Centro", in which all the centres spread throughout the historic part of the city are brought together. The UGR's policy of using buildings of historical and cultural value has enriched its heritage, as well as promoting the restoration and maintenance of these buildings. In addition to this emphasis on more traditional elements, the Health Science Technological Park, which is still being developed, demonstrates our strong commitment to innovation by promoting interaction with technological bio-health companies and favouring high-quality healthcare and biomedical knowledge. There are two other UGR Campuses in the cities of Ceuta and Melilla, in Northern Africa.

Over 60,000 undergraduate and postgraduate students study at the UGR, with another 20,000 students taking additional courses, language courses, summer courses etc. The University employs 3650 lecturers and over 2000 administration, technical and maintenance staff.

At present, courses for 75 different qualifications are taught in the 28 teaching centres of the UGR. The courses are taught across 116 departments. The Postgraduate School offers 68 master's courses, 116 doctorate programmes and 113 additional courses.

The commitment to high-quality research has placed the Universidad de Granada in a prominent position in terms of national rankings.The financing of 346 research groups illustrates this commitment.Through the Spanish Research Programme, as well as other national programmes and organisations, the University supports 165 research projects, and the Ministry of Innovation, Science and Business has provided financial support to a high number of Projects of Excellence.

For many years, the UGR has promoted a significant international activity through the Vice-Rector's Office for International Relations.

The importance of the presence of international students is most clearly demonstrated by the 606 mobility agreements signed with European Higher Education institutions and the ERASMUS mobility programmes; the UGR is the leading European university in terms of receiving students and the second Spanish university in terms of the mobility of its own students.

The University is also involved in major exchange programmes with universities in the United States, Canada, Latin America, Central and Eastern Europe, the Middle East, Mediterranean countries, Australia, Oceania and Asia.

About IMSE/University of Sevilla (please see ESSCIRC Programme, page 3).

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ESSDERC SCHEDULE

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Technical Sessions

9:00	**Joint Plenary Lecture**
9:50	**Joint Plenary Lecture**
10:40	**Coffee Break**
11:00	**Fringe Poster Briefing Session**
11:20	**ESSDERC Sessions**
13:00	**Lunch**
14:20	**Fringe Poster Briefing Session**
14:50	**ESSDERC Sessions**
15:50	**ESSDERC Plenary Lecture**
16:50	**Coffee Break**
17:20	**ESSDERC Sessions**
18:40	**Fringe Poster Briefing Session**

Welcome Reception

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Technical Sessions

9:00	**Joint Plenary Lecture**
9:50	**Joint Plenary Lecture**
10:40	**Coffee Break**
11:20	**ESSDERC Sessions**
13:00	**Lunch**
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15:50	**ESSDERC Plenary Lecture**
16:50	**Coffee Break**
17:20	**ESSDERC Sessions**

Gala Dinner

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Technical Sessions

9:00	**Joint Plenary Lecture**
9:50	**Joint Plenary Lecture**
10:40	**Coffee Break**
11:20	**ESSDERC Sessions**

13:00	**Lunch**
14:50	**ESSDERC Sessions**
15:50	**ESSDERC Plenary Lecture**
16:50	**Coffee Break**
17:20	**ESSDERC Sessions**

Friday, September 17th, 2010

Workshops
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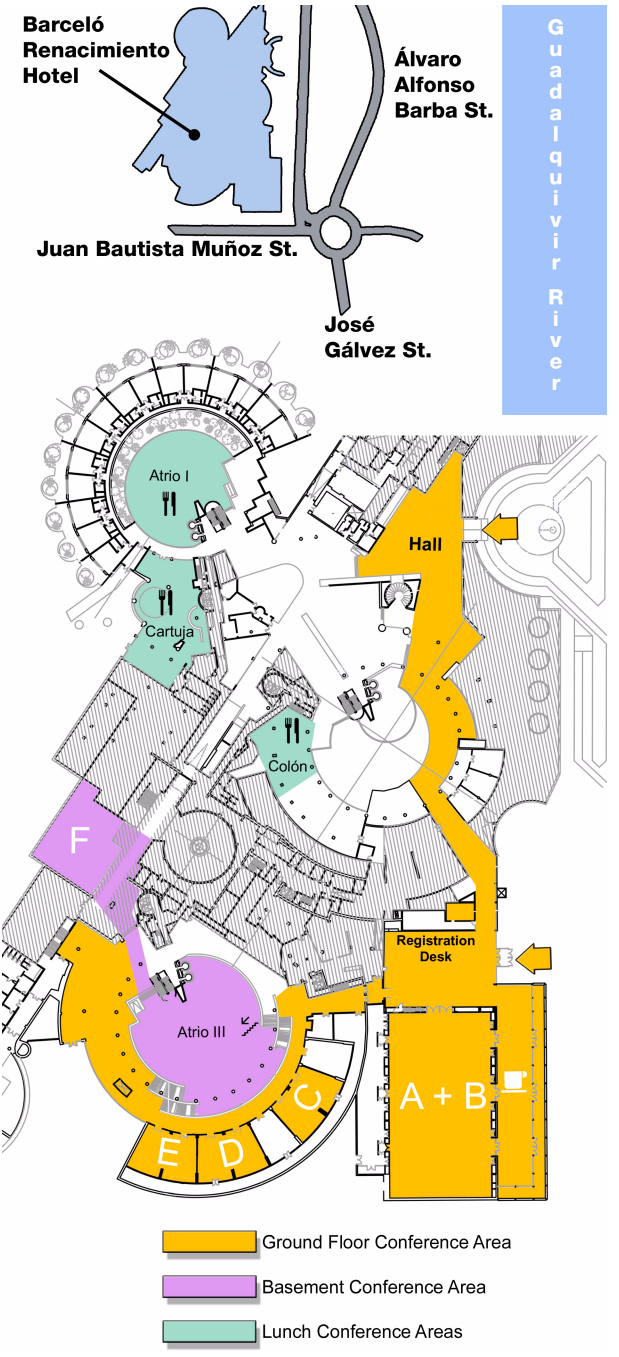
MEETING ROOMS FLOORPLAN



Tuesday September 14th, 2010

Time	ROOM B	ROOM E	ROOM D	ROOM A	ROOM C	ROOM F
8:30	CONFERENCE OPENING (Prof. Ángel Rodríguez-Vázquez and Prof. José Luís Huertas) ROOM A+B					
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09:50-10:40	A2L-A (ROOM A+B) JOINT PLENARY: 3D Integration Technology: Status and Application Development SPEAKER: Dr. Peter Ramm (Fraunhofer IZM Munich Division)					
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11:00-11:20	FRINGE POSTER BRIEFING SESSION					
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14:50-15:50	A4L-B Alternative FETs	A4L-C Special characterization methods and structures	A4L-D Advances in algorithms and simulation methods	A4L-A (ROOM A) ESSCIRC PLENARY: Terahertz Imaging with CMOS/BiCMOS Process Technologies SPEAKER: Dr. Ullrich Pfeiffer (University of Wuppertal, Germany)		
15:50-16:50	A5L-A (ROOM B) ESSDERC PLENARY: GaN-on-Si Technology, A New Approach for Advanced Devices SPEAKER: Dr. Tomás Palacios (Massachusetts Institute of Technology, USA)			A5L-F Amplifiers I	A5L-G Micropower AD interfaces	A5L-H mm-Wave Transceivers
16:50-17:20	COFFEE BREAK					
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Wednesday September 15th, 2010

Time	ROOM B	ROOM E	ROOM D	ROOM A	ROOM C	ROOM F
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09:50-10:40	B2L-A (ROOM A+B) JOINT PLENARY: Energy Harvesting - from Devices to Systems SPEAKER: Dr. Yiannos Manoli (IMTEK - University of Freiburg and HSG-IMIT)					
10:40-11:20	COFFEE BREAK					
11:20-13:00	B3L-B Simulation of advanced silicon devices	B3L-C Photodetectors	B3L-D Silicon and Gallium Nitride power devices	B3L-F TDCs and Timing Circuits	B3L-G Sensors	B3L-H Power Amplifiers
13:00-14:50	LUNCH					
14:50-15:50	B4L-B Modeling of temperature and stress impacts	B4L-C Advanced FET characterization	B4L-D Phase Change Memories	B4L-A (ROOM A) ESSCIRC PLENARY: Analog Mixed-Signal Circuits in Advanced Nano-scale CMOS Technology SPEAKER: Dr. Ian Young (Intel Corporation)		
15:50-16:50	B5L-A (ROOM B) ESSDERC PLENARY: High Power LEDs for Solid State Lighting SPEAKER: Dr. Berthold Hahn (Osram Opto Semiconductors)			B5L-F Amplifiers II	B5L-G Circuits for Implantable Devices	B5L-H mm-Wave Receivers
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17:20-18:40	B6L-B Leakage current and traps	B6L-C Tunneling FET devices	B6L-E Memories	B6L-F Pipeline ADCs	B6L-G Biomedical Applications	B6L-H RF Building Blocks
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09:50-10:40	C2L-A (ROOM A+B) JOINT PLENARY: FDSOI: From Materials to Devices and Circuit Applications SPEAKER: Dr. Carlos Mazuré (SOITEC)					
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14:50-15:50	C4L-B Channel and Gate Stack Engineering	C4L-C Simulation of III/V devices	C4L-D Charge Trap NAND Flash	C4L-A (ROOM A) ESSCIRC PLENARY: Ultra Low Power and Miniaturized MEMS-based Radio for BAN and WSN Applications SPEAKER: Dr. David Ruffieux (Swiss Center for Electronics and Microtechnology CSEM, Switzerland)		
15:50-16:50	C5L-A (ROOM B) ESSDERC PLENARY: Trends & Perspectives for Electrical Characterization & Reliability Assessment SPEAKER: Dr. Guido Groeseneken (IMEC)		C5L-E Emerging Memories	C5L-F mm-wave radar and imaging		C5L-H UWB Communications
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17:20-18:40	C6L-B Analytical/compact models	C6L-C Electromechanical Devices	C6L-E Circuit Design in Emerging Technologies	C6L-F Signal Processing Platforms		C6L-H Optical Communications

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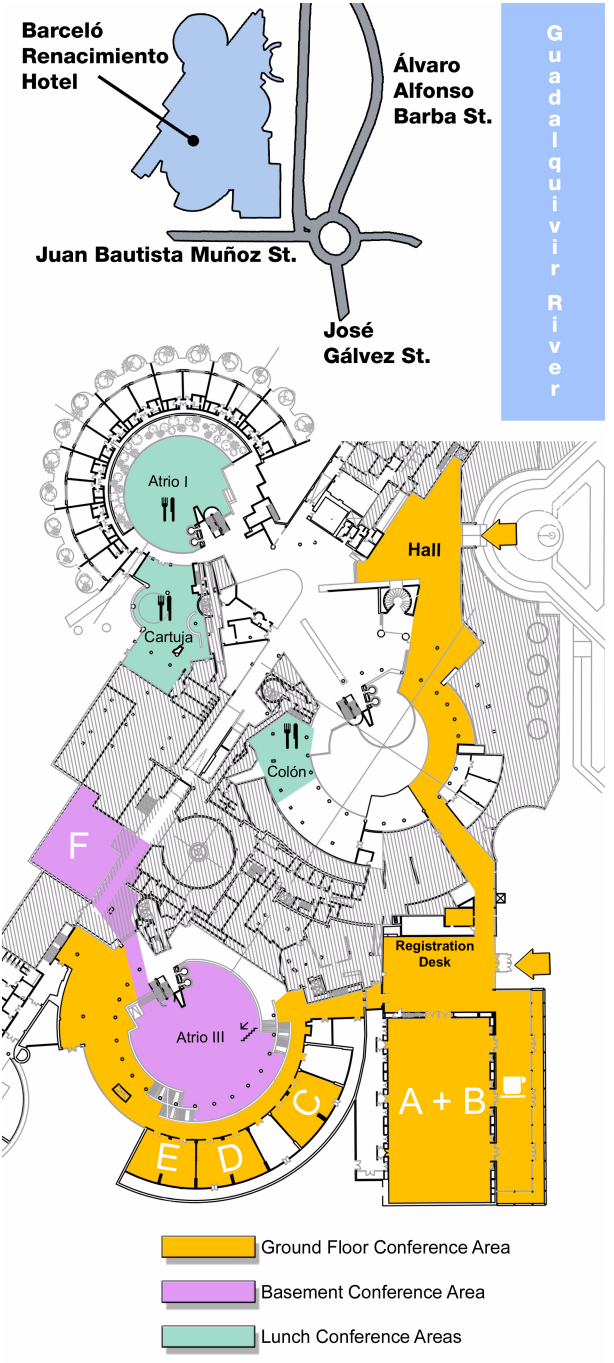
CONFERENCE VENUE



CONFERENCE OVERVIEW

In addition to contributed papers and plenary lectures, the event will include tutorials, exhibits and satellite workshops to be organized before and after the conference.
An attractive social program will complement the event, featuring a welcome reception, a gala dinner with awards ceremony, and excursions.

SCHEDULE AT A GLANCE
MONDAY, SEPTEMBER 13TH, 2010 Tutorials
TUESDAY, SEPTEMBER 14TH, 2010 Conference Opening Technical Sessions Welcome Reception
WEDNESDAY, SEPTEMBER 15TH, 2010 Technical Sessions Gala Dinner
THURSDAY, SEPTEMBER 16TH, 2010 Technical Sessions
FRIDAY, SEPTEMBER 17TH, 2010 Workshops

THE AIM OF THE CONFERENCE

The aim of the ESSDERC conference is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and technologies.

GENERAL SCOPE OF THE CONFERENCE

ESSDERC and its sister conference ESSCIRC, which deals with solid-state circuits, are governed by a single Steering Committee. The increasing level of integration for system-on-chip design made available by advances in silicon technology is stimulating more than ever before the need for deeper interaction among technologists, device experts, and circuit and system designers.
While keeping separate Technical Program Committees, ESSDERC and ESSCIRC will share Plenary Keynote Presentations and Joint Sessions bridging both communities. Attendees registered for either conference are encouraged to attend any of the scheduled parallel sessions.

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Themes of the conference

The main themes for original contributions to be submitted to ESSDERC 2010 include, but are not limited to the following:

Advanced CMOS Devices

Ultimate CMOS scaling, high performance, low power and low voltage devices, novel MOS device architectures, high-mobility channel engineered devices, SOI, SGOI, and SiON devices; SiGe, Ge, and strained devices. 3D integrated circuits.

Process & Integration

Front-end and back-end processes for fabrication of logic memory and 3D integrated circuits; advances in integration for ULSI; advanced/novel memory process integration; logic and mixed-mode IC manufacturing; RF integration; photonics integration.

Telecommunication

RF CMOS, analog and mixed signal devices, passives, antennas, filters, RF MEMS, Bipolar, BiCMOS, compound semiconductors and alloys; optoelectronic devices; integrated RF components: inductors, capacitors, and switches.

Power Devices

Smart power devices, high-voltage, high power devices, high temperature operation, SiC devices, CMOS compatible power devices, IC cooling. Discrete and integrated high power/current/voltage devices.

Modeling and Simulation

Numerical, analytical and statistical modeling of solid-state electronic and optoelectronic devices; compact circuit modeling for devices and interconnects, simulation of front-end and back-end fabrication processes, electro-thermal modeling.

Characterization, Reliability and Yield

Characterization techniques, parameter extraction, advanced test structures and methodologies, reliability issues for new materials and devices; reliability of advanced interconnects, ESD, soft errors, noise and mismatch behavior.

Memories

Novel memory cell concepts, embedded and stand-alone memories, DRAM, FeRAM, MRAM, PCRAM, CBRAM, Flash, SONOS, nanocrystal memories, single and few electron memories, 3D IC stacks, organic memories, 3D integration, reliability and modeling.

MEMS, DISPLAYS AND SOC

Design, fabrication, modeling, reliability and packaging of all physical sensors and MEMS categories: bio-sensors for chemical, molecular and biological applications, devices and technologies for lab-on-chip, integration of detectors, sensors, and actuators, CCDs and CMOS imagers, optical on chip communication.

EMERGING NON-CMOS DEVICES AND TECHNOLOGIES

Nanotubes, nanowires and nanoparticles for electronic, optoelectronic and sensor applications. New device characterization techniques and performance evaluation methodologies.

GaN-on-Si Technology, A New Approach for Advanced Devices

Dr. Tomás Palacios, Massachusetts Institute of Technology

Tomás Palacios, Massachusetts Institute of Technology, United States
J. W. Chung, Massachusetts Institute of Technology, United States
K. Ryu, Massachusetts Institute of Technology, United States
B. Lu, Massachusetts Institute of Technology, United States

Abstract

The Si substrate of GaN-on-Si wafers offers new opportunities to increase the functionality and performance of nitride-based devices. This paper will review three examples of these new devices/systems. First, GaN-on-Si substrates allow the on-chip heterogeneous integration of GaN and Si electronics.

Second, the easy removal of the Si substrate through dry or wet etching gives access to the N-face of the GaN layer, and all the new device structures that this orientation enables. Finally, the use of Si substrates for the growth of GaN high voltage switches makes the cost of these devices competitive with Si devices, and the total or partial etch of Si brings a new degree of freedom to increase the breakdown and performance of GaN transistors.

Dr. Tomás Palacios is an Associate Professor in the Department of Electrical Engineering and Computer Science at the Massachusetts Institute of Technology, where he leads the Advanced Semiconductor Materials and Devices Group. He received his Ph.D. in Electrical Engineering from the University of California - Santa Barbara, and a M.Sc. degree from the Polytechnical University of Madrid, Spain. His research focuses on the development of new electronic devices to advance the fields of information technology, energy conversion and biosensors. He is especially interested in expanding the frequency performance of GaN transistors and developing new devices and circuits based on graphene. His work has been recognized with multiple awards including, the 2010 Young Scientist Award of the International Symposium on Compound Semiconductors (ISCS), the 2009 NSF CAREER Award, the 2009 ONR Young Investigator Award, the 2008 DARPA Young Faculty Award, the 2006 UCSB Lancaster Award, the Young Researcher Award at the 6th International Conference on Nitride Semiconductors, the European Prize

Salva i Campillo, and several best papers awards. Prof. Palacios has authored more than 100 contributions on advanced semiconductor devices in international journals and conferences, 35 of them invited, 3 book chapters and 8 patents.

HIGH POWER LEDS FOR SOLID STATE LIGHTING

Dr. Berthold Hahn, OSRAM

Abstract

For solid stated lighting high light output in combination with high conversion efficacy is essential. High efficiencies are relatively easy to realize at low current densities, but efficiency tends to decline as the current is cranked up. In order to overcome the barriers for high flux LEDs, both epitaxy and chip design have to be optimized.

In this paper we report on the improvement of ThinGaN®-PowerLED structures in epitaxy, chip design, phosphor efficiency and package design. A key for improving LED performance is understanding the carrier loss mechanisms in blue and green epitaxy structures. Assuming an indirect Auger effect as one of the major loss mechanisms in InGaN LEDs, a reduction of the carrier density per emitting well is enabling efficiency improvement for blue/green LEDs.

Along with improved epi designs the extraction efficiency had to be improved. A new chip design allows high current operation in combination with efficiencies beyond 100lm/W for white. New conversion schemes allow the fabrication of extremely efficient green light sources, which enable new generations of high flux projection applications.

Dr. Berthold Hahn received his PhD in physics from Regensburg University at 1998.

Dr. Hahn is responsible for chip R&D at OSRAM Opto Semiconductors for visible and infrared LEDs. He joined OSRAM Opto Semiconductors in 1998. He was responsible for the epi development of InGaN-based LEDs. He headed the ThinGaN programand took over responsibility for nitride-based high-power chip development. Since 2008 he has also been responsible for R&D of AlInGaP- and AlGaAs-based LEDs.

TRENDS AND PERSPECTIVES FOR ELECTRICAL CHARACTERIZATION AND RELIABILITY ASSESSMENT IN ADVANCED CMOS DEVICES AND TECHNOLOGIES

Dr. Guido Groeseneken, IMEC

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Robin Degraeve, IMEC, Belgium
Ben Kaczer, IMEC, Belgium
Koen Martens, IMEC, Belgium

Abstract

In this paper we give a brief historical review of the evolution of device reliability research over the past decades.
Then we give some examples on how established characterization techniques that were developed for silicon based devices can be completely misinterpreted when applied to Ge or III-V based MOS-structures, and how a simple modification of the technique can ensure a correct interpretation. We also show how novel techniques, such as TSCIS (Trap spectroscopy by Charge Injection and Sensing). were developed recently to overcome the problem of dielectric material screening for logic and memory applications. With the scaling of the devices into the nanometer regime single traps are causing large variations in the device parameters, which leads to a time-dependent variability, which makes lifetime analysis difficult. Finally we show that when using the classical reliability assessment methodology based on accelerated testing, the available reliability margins are strongly reduced, in some cases even down to zero, especially for sub-1nm EOT (Effective Oxide Thickness) devices. As a result, we argue that the reliability community will have to look for alternative ways to ensure and guarantee the lifetime of future products.

Dr. Guido Groeseneken received the M.Sc. degree in electrical engineering (1980) and the Ph.D degree in applied sciences (1986), both from the Katholieke Universiteit Leuven, Belgium. In 1987 he joined the R&D Laboratory of IMEC (Interuniversity Microelectronics Center) in Leuven, Belgium, where he is responsible for research in reliability physics for deep submicron CMOS technologies. From October 2005 until April 2007 he was also responsible for the IMEC Post CMOS Nanotechnology program within IMEC's core partner research program. Since 2001 he is Professor at the KU Leuven, where he is Program Director of the Master in Nanoscience and Nanotechnology, and where he is also

coordinating a European Erasmus Mundus Master program in Nanoscience and nanotechnology. He became an IEEE Fellow in 2005 and an IMEC Fellow in 2007.

He has made contributions to the fields of non-volatile semiconductor memory devices and technology, reliability physics of VLSI-technology, hot carrier effects in MOSFET's, time-dependent dielectric breakdown of oxides, Negative-Bias-Temperature Instability effects, ESD-protection and -testing, plasma processing induced damage, electrical characterization of semiconductors and characterization and reliability of high k dielectrics. Recently he has also interest in nanotechnology for post-CMOS applications, such as carbon nanotubes for interconnect applications, tunnel FET's for alternative nanowire devices etc.

He has served as a technical program committee member of several international scientific conferences, among which the IEEE International Electron Device Meeting (IEDM), the European Solid State Device Research Conference (ESSDERC), the International Reliability Physics Symposium (IRPS), the IEEE Semiconductor Interface Specialists Conference (SISC) and the EOS/ESD Symposium. From 2000 until 2002 he also acted as European Arrangements Chair of IEDM. In 2005 he was the General Chair of the Insulating Films on Semiconductor (INFOS) conference, organized in Leuven, Belgium.

He has authored or co-authored more than 500 publications in international scientific journals and in international conference proceedings, 6 book chapters and 10 patents in his fields of expertise.

MONDAY, SEPTEMBER 13TH, 2010

TUTORIAL 1: NANOELECTRONICS: A TOOL TO FACE THE FUTURE.

Organisers: Francisco Gámiz and Andrés Godoy, *University of Granada*

Full-Day Tutorial (8:50 - 17:20)

Room D

Content

The aim of this Tutorial is to present the status and trends of different hot topics in the field of nanoelectronics. All the presentations will consist on a 50 minutes oral presentation + 10 minutes of questions.

Agenda

8:50–9:00
Introduction
F. Gámiz, A. Godoy, University of Granada
9:00–10:00
CMOS process variability – from technology to circuits and systems
J. Lorenz, Fraunhofer Institute, Germany
10:00–11:00
Industrial challenges for the CMOS technology to reach the 22nm and 16nm nodes
T. Skotnicki, STMicroelectronics, France
11:00–11:20 BREAK
11:20–12:20
1T-DRAM structures
Sorin Cristoloveanu, IMEP-LAHC, France
12:20–14:00 LUNCH
14:00–15:00
III-V devices for high frequency applications
Tomás Palacios, MIT
15:00–16:00
Silicon nanowires
T. Ernst, CEA-LETI, Grenoble, France
16:00–16:20 BREAK
16:20–17:20
Carbon based Nanoelectronics: Carbon Nanotubes & Graphene as drivers to device innovation and Post-CMOS area
Sthephan Roche, CEA, INAC, SP2M, Grenoble, France

TUTORIAL 2: SILICON ON INSULATOR: MATERIALS TO CIRCUIT DESIGN.

Organiser: Jean-Pierre Colinge, *Tyndall Institute, Cork Ireland*.

Full-Day Tutorial (9:00 - 17:00)

Room E

Content

This tutorial will cover different aspects of SOI technology, ranging form substrate preparation to circuit design. The Smart-Cut® technique has enabled the mass production of SOI wafers, but is also a powerful technique for the formation of hybrid substrates and for More the Moore applications. The particular properties of SOI MOSFETs can be used to improve circuit speed or electrical performance. These properties will be reviewed and compact models for SOI MOSFETs will be presented. Design techniques and tools for analogue, digital and RF applications will be described.

Agenda

9:00-10:00
Smart-cut enabled materials
C Colinge, Tyndall
10:00-11:00
Physics of SOI devices
JP Colinge, Tyndall
11:00-12:00
SOI MOSFET compact models
B Iniguez, URV
12:00-14:00 LUNCH
14:00-15:00
SOI Design: RF
JP Raskin, UCL
15:00-16:00
SOI design: analog
D Flandre, UCL
16:00-17:00
SOI design: logic circuits
Ph Flatresse, STM

For further information about these tutorials, please visit the webpage of the conference at http://www.essderc2010.org/essdercTut.html

TUESDAY SEPTEMBER 14

Process Integration: More than Moore Devices Architectures
(Lecture)

Session Code: A3L-B

Location: Room B

Date & Time: Tuesday September 14, 2010 (11:20 - 13:00)

Chair(s): Francis Balestra
IMEP-LAHC Laboratory, France
Anton Bauer
IISB-Fraunhofer, Germany

11:20 **Silicon Photodiodes for High-Efficiency Low-Energy Electron Detection**
Agata Sakic, Lis Nanver, Tom Scholtes, Carel Heerkens, TU *Delft.* Gerard van Veen, Kees Kooijman, Patrick Vogelsang, *FEI company.*

11:40 **New Mechanism of Plasma Induced Damage on CMOS Image Sensor: Analysis and Process Optimization**
Jean-Pierre Carrere, Jean-Pierre Oddou, Claire Richard, Cecile Jenny, Maxime Gatefait, Sebastien Place, Christophe Aumont, Arnaud Tournier, Francois Roy, *STMicroelectronics.*

12:00 **Drain-Extended MOS Transistors Capable for Operation at 10V and at Radio Frequencies**
Andreas Mai, Holger Rücker, *IHP Innovations for High Performance Microelectronics.*

12:20 **Analysis of Silicon on-Chip Integrated Antennas for Intra- and Inter-Chip Wireless Interconnects**
T. Kikkawa, K. Kimoto S. Kubota, *Hiroshima University.*

12:40 **Passive Components Integration in CMOS Technology**
Siamak Salimy, Fatiha Challali, Antoine Goullet, Marie-Paule Besland, Serge Toutain, Dominique Averty, Ahmed Rhallabi, Jean-Pierre Landesman, *Nantes University.* Jean-Claude Saubat, Alain Charpentier, *MHS Electronics.*

Reliability, variability and mismatch
(Lecture)

Session Code: A3L-C

Location: Room E

Date & Time: Tuesday September 14, 2010
(11:20 - 13:00)

Chair(s): Montserrat Nafría,
UAB Universitat Autònoma de Barcelona, Spain
Reinout Woltjer,
NXP, Netherlands

11:20 **Drain Current Variability in 45nm Heavily Pocket-Implanted Bulk MOSFET**
Cecilia Mezzomo, *STMicroelectronics, IMEP-LAHC.* Aurelie Bajolet, *STMicroelectronics.* Augustin Cathignol, *IBM France.* Gerard Ghibaudo, *IMEP-LAHC.*

11:40 **Mismatch Sources in LDMOS Devices**
Pietro Andricciola, Hans Tuinhout, *NXP Semiconductors.*

12:00 **Combining Process and Statistical Variability in the Evaluation of the Effectiveness of Corners in Digital Circuit Parametric Yield Analysis**
Plamen Asenov, Noor Ain Kamsani, David Reid, Campbell Millar, Scott Roy, Asen Asenov, *University of Glasgow.*

12:20 **Threshold Voltage Shift and Drain Current Degradation by NBT Stress in Si (110) pMOSFETs**
Kensuke Ota, Masumi Saitoh, Yukio Nakabayashi, Takamitsu Ishihara, Toshinori Numata, *Toshiba Corporation.* Ken Uchida, *Tokyo Institute of Technology.*

12:40 **Resistive Switching-Like Behaviour of the Dielectric Breakdown in Ultra-Thin Hf Based Gate Stacks in MOSFETs**
Albert Crespo-Yepes, Javier Martín-Martínez, *Universitat Autònoma de Barcelona.* Aude Rothschild, *IMEC.* Rosana Rodríguez, Montse Nafría, Xavier Aymerich, *Universitat Autònoma de Barcelona.*

TUESDAY SEPTEMBER 14

SRAM and DRAM
(Lecture)

Session Code: A3L-D

Location: Room D

Date & Time: Tuesday September 14, 2010
(11:20 - 13:00)

Chair(s): Barbara De Salvo,
CEA-LETI, France
Andreas Schenk,
ETH Zurich, Switzerland

11:20 **Tri-Gate Bulk CMOS Technology for Improved SRAM Scalability**
Changhwan Shin, *University of California*, *Berkeley*. Chen Hua Tsai, Mei Hsuan Wu, Chung Fu Chang, You Ren Liu, Chih Yang Kao, Guan Shyan Lin, Kai Ling Chiu, Chuan-Shian Fu, Cheng-Tzung Tsai, Chia Wen Liang, *United Microelectronics Corporation*. Borivoje Nikolic, Tsu-Jae King Liu, *University of California, Berkeley*.

11:40 **Impact of Fast-Recovering NBTI Degradation on Stability of Large-Scale SRAM Arrays**
Stefan Drapatz, *TU München.* Karl Hofmann, Georg Georgakos, *Infineon Munich.* Doris Schmitt-Landsiedel, *TU München.*

12:00 **Experimental Comparison of Programming Mechanisms in 1T-DRAM Cells with Variable Channel Length**
Alexandre Hubert, *CEA Leti Minatec.* Maryline Bawedin, *IMEP, INPG-Minatec.* Georges Guegan, *CEA Leti Minatec.* Sorin Cristoloveanu, *IMEP, INPG-Minatec.* Thomas Ernst, *CEA Leti Minatec.* Olivier Faynot, *CEA Leti Minatec.*

12:20 **Substrate Bias Dependency of Sense Margin and Retention in Bulk FinFET 1T-DRAM Cells**
Nadine Collaert, Marc Aoulaiche, An De Keersgieter, Bart De Wachter, Malgorzata Jurczak, Laith Altimime, *IMEC.*

12:40 **COLK cell: A new embedded DRAM architecture for advanced CMOS nodes**
Sébastien Cremer, Olivier Goducheau, Hervé Petiton, Sébastien Gaillard, Emek Yesilada, Marc Vernet, Cécile Jenny, Frédéric Lalanne, *STMicroelectronics.*

TUESDAY SEPTEMBER 14

Alternative FETs
(Lecture)

Session Code: A4L-B

Location: Room B

Date & Time: Tuesday September 14, 2010 (14:50 - 15:50)

Chair(s): Nadine Collaert, *IMEC, Belgium*
Thanasis Dimoulas, *Demokritos, Greece*

14:50 **Sub-60nm Si Tunnel Field Effect Transistors with I_{on} > 100µA/ µm**
Wei Yip Loh, *SEMATECH.* Kanghoon Jeon, *SEMATECH/University of California Berkeley.* Chang Yong Kang, Jungwoo Oh, *SEMATECH.* Pratik Patel, *University of California Berkeley.* Casey Smith, Joel Barnett, Chanro Park, *SEMATECH.* Tsu-Jae King Liu, *University of California Berkeley.* Hsing-Huang Tseng, *Texas State University.*Prashant Majhi, *SEMATECH Intel.* Raj Jammy, *SEMATECH.* Chenming Hu, *University of California Berkeley.*

15:10 **High-Performance Enhancement-Mode $In_{0.53}Ga_{0.47}As$ Surface Channels n-MOSFET with Thin $In_{0.2}Ga_{0.8}As$ capping and Laser anneal effect**
Injo Ok, Pui-Yee Hung, Dmitry Veksler, Jungwoo Oh, Prashant Majhi, Raj Jammy, *SEMATECH.*

15:30 **Optimization of Tunnel FETs: Impact of Gate Oxide Thickness, Implantation and Annealing Conditions**
Daniele Leonelli, *IMEC /KU Leuven.* Anne Vandooren, Rita Rooyackers, *IMEC.* Stefan De Gendt, Marc Heyns, Guido Groeseneken, *IMEC/KU Leuven.*

TUESDAY SEPTEMBER 14

Special characterization methods and structures
(Lecture)

Session Code: A4L-C

Location: Room E

Date & Time: Tuesday September 14, 2010 (14:50 - 15:50)

Chair(s): Sorin Cristoloveanu, *IMEP-LAHC, France*

14:50 **Test Structure and Method for the Experimental Investigation of Internal Voltage Amplification and Surface Potential of Ferroelectric MOSFETs**
Alexandru Rusu, Giovanni Salvatore, Adrian Ionescu, EPFL *Ecole Polytechnique Federale de Lausanne.*

15:10 **Experimental Evidence of Unconventional Room-Temperature Quantum Hall Effect (RTQHE) in 65nm Si nMOSFETs at Very Low Magnetic Fields**
Edmundo Gutiérrez-D., *INAOE.* Fernando Guarin, *IBM Microelectronics.*

15:30 **Thermal Broadening of Two-Dimensional Electron Gas Mobility Distribution in AlGaN/AlN/GaN Heterostructures**
Gilberto A. Umana-Membreno, *The University of Western Australia.* Tiziana Stomeo, Vittorianna Tasco, Adriana Passaseo, Massimo De Vittorio, *CNR-NANOSCIENZE.* Lorenzo Faraone, *The University of Western Australia.*

TUESDAY SEPTEMBER 14

Advances in algorithms and simulation methods
(Lecture)

Session Code: A4L-D

Location: Room D

Date & Time: Tuesday September 14, 2010
(14:50 - 15:50)

Chair(s): Jürgen Lorenz,
IISB-Fraunhofer, Germany

14:50 **Hardware/Software Co-Simulation for the Rapid Prototyping of an Acceleration Sensor System with Force-Feedback Control**
Ruslan Khalilyulin, Thomas Steinhuber, Gabriele Schrag, Gerhard Wachutka, TU *München.*

15:10 **On the Inclusion of Lorentz Force Effects in TCAD Simulations**
Wim Schoenmaker, Peter Meuris, *MAGWEL NV.*
Jean Jimenez, Philippe Galy, *STMicroelectronics.*

15:30 **Modeling Methodology of High-Voltage Substrate Minority and Majority Carrier Injections**
Fabrizio Lo Conte, Jean-Michel Sallese, Maher Kayal, EPFL *Ecole Polytechnique Federale de Lausanne.*

TUESDAY SEPTEMBER 14

SOI MOSFETs
(Lecture)

Session Code: A6L-B

Location: Room B

Date & Time: Tuesday September 14, 2010
(17:20 - 18:40)

Chair(s): Kazunari Ishimaru,
Toshiba, Japan
Carlos Mazuré,
SOITEC, France

17:20 **Subthreshold FinFET SRAM Cell Optimization Considering Surface-Orientation Dependent Variability**
Ming-Long Fan, Vita Pi-Ho Hu, Chien-Yu Hsieh, Pin Su, Ching-Te Chuang, *National Chiao Tung University.*

17:40 **Fin-Height Controlled PVD-TiN Gate FinFET SRAM for Enhancing Noise Margin**
Yongxun Liu, K. Endo, Shin-Ichi O'Uchi, Junichi Tsukada, Hiromi Yamauchi, Yuki Ishikawa, Kunihiro Sakamoto, Takashi Matsukawa, Meishoku Masahara, *Nanoelectronics Research Institute of AIST.* T. Kamei, T. Hayashida, A. Ogura, *Meiji University.*

18:00 **Dual Channel and Strain for CMOS Co-Integration in FDSOI Device Architecture**
Cyrille Le Royer, Mikaël Cassé, François Andrieu, Olivier Weber, Laurent Brevard, Pierre Perreau, Jean-François Damlencourt, Sophie Baudot, Claude Tabone, Fabienne Allain, Pascal Scheiblin, Caroline Rauer, Louis Hutin, *CEA Leti Minatec.* C. Figuet, C. Aulnette, N. Daval, B.-Y. Nguyen and K. K. Bourdelle, *SOITEC.*

18:20 **UT2B-FDSOI Device Architecture Dedicated to Low Power Design Techniques**
Jean-Philippe Noel, Olivier Thomas, Marie-Anne Jaud, *CEA-Leti.* Claire Fenouillet-Beranger,*CEA-Leti/ STMicroelectronics.* Pierrette Rivallin, Pascal Scheiblin, Thierry Poiroux, *CEA-Leti.* Frédéric Boeuf, *STMicroelectronics.* François Andrieu, Olivier Weber, Olivier Faynot, *CEA-Leti.* Amara Amara, ISEP.

Ferromagnetic and polycrystalline devices
(Lecture)

Session Code: A6L-C

Location: Room E

Date & Time: Tuesday September 14, 2010
(17:20 - 18:40)

Chair(s): Steve Hall,
University of Liverpool, UK
Ryoichi Ishihara,
TU Delft, Netherlands

17:20 **Ultra-low Volume Ferromagnetic Nanodots for Field-coupled Computing Devices**
Josef Kiermaier, Stephan Breitkreutz, Xueming Ju, *TU München.* Gyorgy Csaba, *University of Notre Dame.* Doris Schmitt-Landsiedel, Markus Becherer, *TU München.*

17:40 **The Curie Temperature As a Key Design Parameter of Ferroelectric Field Effect Transistors**
Giovanni Antonio Salvatore, Livio Lattanzio, Didier Bouvet, Adrian M. Ionescu, EPFL *Ecole Polytechnique Federale de Lausanne.*

18:00 **Performance Trade-Offs in Polysilicon Source-Gated Transistors**
Radu Sporea, *University of Surrey.* Mike Trainor, Nigel Young, *Philips Research.* John Shannon, Ravi Silva, *University of Surrey.*

18:20 **Analysis and Modeling of Pseudo-Short-Channel Effects in ZnO-Nanoparticle Thin-Film Transistors**
Karsten Wolff, Ulrich Hilleringmann, *University of Paderborn.*

WEDNESDAY SEPTEMBER 15

Simulation of advanced silicon devices
(Lecture)

Session Code: B3L-B

Location: Room B

Date & Time: Wednesday September 15, 2010 (11:20 - 13:00)

Chair(s): Bernd Meinerzhagen, *Technical University of Braunschweig, Germany*
Massimo Rudan, *University of Bologna, Italy*

11:20 **Comparison of Strained SiGe Heterostructure-on-Insulator (001) and (110) PMOSFETs: C-V Characteristics, Mobility and ON Current**
Anh-Tuan Pham, *Technical University of Braunschweig.* Christoph Jungemann, *Bundeswehr University in Munich.* Bernd Meinerzhagen, *Technical University of Braunschweig.*

11:40 **A New Model for the Backscatter Coefficient in Nanoscale MOSFETs**
Jan-Laurens van der Steen,*University of Twente.* Pierpaolo Palestri, David Esseni, *University of Udine.* Ray Hueting, *University of Twente.*

12:00 **Multi-Subband Monte Carlo Simulation of Bulk MOSFETs for the 32nm-Node and Beyond**
Carlos Sampedro, Francisco Gámiz, Andrés Godoy, *University of Granada.* Raúl Valín, Antonio García-Loureiro, *University of Santiago de Compostela.* Noel Rodríguez, *University of Granada.*

12:20 **Modeling Study on Carrier Mobility in Ultra-Thin Body FinFETs with Circuit-Level Implications**
Mirko Poljak, *University of Zagreb.* Vladimir Jovanovic,*TU Delft/University of Zagreb.* Tomislav Suligoj, *University of Zagreb.*

12:40 **TCAD Based Device Architecture Exploration Towards Half-Terahertz Silicon/Germanium Heterojunction Bipolar Technology**
Arturo Sibaja-Hernández, Shuzhen You, Stefaan Van Huylenbroeck, Rafael Venegas, Kristin De Meyer, Stefaan Decoutere, *IMEC.*

WEDNESDAY SEPTEMBER 15

Photodetectors
(Lecture)

Session Code: B3L-C

Location: Room E

Date & Time: Wednesday September 15, 2010 (11:20 - 13:00)

Chair(s): Anthony O'Neill, *New Castle University, UK*
Mervin Armstrong, *Queen´s University Belfast, UK*

11:20 **Integrated Phototransistors in a CMOS Process for Optoelectronic Integrated Circuits**
Plamen Kostov, Wolfgang Gaberl, Horst Zimmermann, *Vienna University of Technology.*

11:40 **CMOS Process Enhancement for High Precision Narrow Linewidth Applications**
Frank Hochschulz, Uwe Paschen, Holger Vogt, *Fraunhofer IMS.*

12:00 **A 2µm Diameter, 9Hz Dark Count, Single Photon Avalanche Diode in 130nm CMOS Technology**
Justin Richardson, Lindsay Grant, *STMicroelectronics.* Eric Webster, Robert Henderson, *University of Edinburgh.*

12:20 **Buried Finger Concept for a Correlating Double Cathode Photodetector in BiCMOS**
Alexander Nemecek, *University of Applied Sciences Wr. Neustad/t/Vienna University of Technology.* Horst Zimmermann, *Vienna University of Technology.*

12:40 **Understanding Dark Current in Pixels of Silicon Photomultipliers**
Roberto Pagano, Salvatore Lombardo, Sebania Libertino, *CNR.* Giuseppina Valvo, Giovanni Condorelli, Beatrice Carbone, Delfo Nunzio Sanfilippo, Piero Giorgio Fallica, *ST Microelectronics.*

WEDNESDAY SEPTEMBER 15

Silicon and Gallium Nitride power devices
(Lecture)

Session Code: B3L-D

Location: Room D

Date & Time: Wednesday September 15, 2010 (11:20 - 13:00)

Chair(s): Marie Denison, *Texas Instruments, USA*
Gerhard Wachutka, *TU München, Germany*

11:20 **Hot-Carrier Stress Induced Degradation in Multi-STI-Finger LDMOS: an Experimental and Numerical Insight**
Stefano Poli, Alberto Loi, Susanna Reggiani, Giorgio Baccarani, Elena Gnani, Antonio Gnudi, *University of Bologna.* Marie Denison, Sameer Pendharkar, Rick Wise, Sridhar Seetharaman, *Texas Instruments.*

11:40 **Repetitive Avalanche Cycling of Low-Voltage Power Trench N-MOSFETs**
Olayiwola Alatise, Ian Kennedy, George Petkos, Keith Heppenstall, Khalid Khan, Adrian Koh, Phil Rutter, *NXP Semiconductors.*

12:00 **Investigation of a Dual Channel N/P-LDMOS and Application to LDO Linear Voltage Regulation**
Marie Denison, Yizhong Xie, Hannes Estl, *Texas Instruments.*

12:20 **High Transconductance A1GaN/GaN HEMT with Thin Barrier on Si(111) Substrate**
Francois Lecourt, Douvry Yannick, Nicolas Defrance, Virginie Hoel, Jean-Claude De Jaeger, *IEMN.* Samira Bouzid, M. Renvoise, Derek Smith, Hassan Maher, *OMMIC.*

12:40 **Study of GaN HEMTs Electrical Degradation by Means of Numerical Simulations**
Valerio Di Lecce, Michele Esposto, Matteo Bonaiuti, Fausto Fantini, Alessandro Chini, *Universitá di Modena e Reggio Emilia.*

WEDNESDAY SEPTEMBER 15

Modeling of temperature and stress impacts
(Lecture)

Session Code: B4L-B

Location: Room B

Date & Time: Wednesday September 15, 2010 (14:50 - 15:50)

Chair(s): Herve Jaouen, *STMicroelectronics, France*

14:50 **On the Influence of Flash Peak Temperature Variations on Schottky Contact Resistances of 6-T~SRAM~Cells**
Christian Kampen, Alexander Burenkov, Jürgen Lorenz, *Fraunhofer IISB.*

15:10 **Temperature Dependent Dielectric Absorption Characterization and Modeling for SiN, Al_2O_3 and Ta_2O_5**
Hajro Muminovic, Philipp Riess, Peter Baumgartner, *Infineon.* Peter Klein, *Hochschule München*.

15:30 **Strained MOSFETs on Ordered SiGe Dots**
Johann Cervenka, Hans Kosina, Siegfried Selberherr, *Institute for Microelectronics TU Wien.* Jianjun Zhang, Nina Hrauda, Julian Stangl, Guenther Bauer, *Johannes Kepler University.* Guglielmo Vastola, Anna Marzegalli, Leo Miglio, *University of Milano-Bicocca.*

WEDNESDAY SEPTEMBER 15

Advanced FET characterization
(Lecture)

Session Code: B4L-C

Location: Room E

Date & Time: Wednesday September 15, 2010 (14:50 - 15:50)

Chair(s): Noel Rodríguez, *University of Granada, Spain*

14:50 **Optimized Oxygen Annealing Process for V_{th} Tuning of p-MOSFET with High-k/Metal Gate Stacks**
Takamasa Kawanago, Yeonghun Lee, Kuniyuki Kakushima, Perhat Ahmet, Kazuo Tsutsui, Akira Nishiyama, Nobuyuki Sugii, Kenji Natori, Takeo Hattori, Hiroshi Iwai, *Tokyo Institute of Technology.*

15:10 **Experimental Analysis of Surface Roughness Scattering in FinFET Devices**
Jae Woo Lee, Doyoung Jang, *IMEP-LAHC & Korea University.* Mireille Mouis, *IMEP-LAHC.* Gyu Tae Kim, *Korea University.* Thomas Chiarella, Thomas Hoffmann, *IMEC.* Gérard Ghibaudo, *IMEP-LAHC.*

15:30 **Parameter Extraction of Nano-Scale MOSFETs Using Modified Y Function Method**
Subramanian Narasimhamoorthy, Gérard Ghibaudo, Mireille Mouis, *IMEP-LAHC.*

WEDNESDAY SEPTEMBER 15

Phase Change Memories
(Lecture)

Session Code: B4L-D

Location: Room D

Date & Time: Wednesday September 15, 2010 (14:50 - 15:50)

Chair(s): Roberto Bez, *Numonyx, Italy*

14:50 **Carbon-Doped GeTe Phase-Change Memory Featuring Remarkable Reset Current Reduction**
Giovanni Betti Beneventi, *CEA-LETI MINATEC/Universitá di Modena e Reggio Emilia.* Luca Perniola, Andrea Fantini, Denis Blachier, Alain Toffoli, *CEA-LETI MINATEC.* Emmanuel Gourvest, *STMicroelectronics/CEA-LETI.* Sylvain Maitrejean, Veronique Sousa, Carine Jahan, Jean-François Nodin, Alain Persico, Sebastien Loubriat, Anne Roule, *CEA-LETI MINATEC. S. Lhostis, CEA-LETI/STMicroelectronics. H. Feldis., G. Reimbold, T. Billon., B. De Salvo, CEA-LETI MINATEC. L. Larcher, P. Pavan, Universitá di Modena e Reggio Emilia. D. Bensahel, P. Mazoyer, R. Annunziata, STMicroelectronics. F. Boulanger, CEA-LETI MINATEC.*

15:10 **Current Distributions of BJT-Based Decoding Array for Phase Change Memory**
Domenico Ventrice, Alessandro Calderoni, Paolo Fantini, *Numonyx.*

15:30 **SET Switching Effects on PCM Endurance**
Vincenzo Della Marca, Francesca Carboni, Luca Larcher, Andrea Padovani, Paolo Pavan, *Universitá di Modena e Reggio Emilia.*

WEDNESDAY SEPTEMBER 15

Leakage current and traps
(Lecture)

Session Code:	B6L-B
Location:	Room B
Date & Time:	Wednesday September 15, 2010 (17:20 - 18:40)
Chair(s):	Stefan Bengtsson, *Chalmers, Sweden* Henryk Przewlocki, *TU-Warsaw,Poland*

17:20 **Study of N-Induced Traps Due to Nitrided Metal Gate in HK/MG nMOSFETs**
Mikaël Cassé, Xavier Garros, Olivier Weber, François Andrieu, Gilles Reimbold, Fabien Boulanger, *CEA-LETI Minatec.*

17:40 **Carbon Junction Implant: Effect on Leakage Currents and Defect Distribution**
Guntrade Roll, Stefan Jakschik, *Namlab gGmbH.* Matthias Goldbach, *Qimonda Dresden.* Thomas Mikolajick, *Namlab gGmbH/University of Dresden.* Lothar Frey, *Fraunhofer IISB.*

18:00 **Grain Boundary-Driven Leakage Path Formation in HfO_2 Dielectrics**
Gennadi Bersuker, Jung Yum, *SEMATECH.* Vanessa Iglesias, Marc Porti, Montse Nafría, UAB *Universitat Autònoma de Barcelona.* Keith McKenna, Alex Shluger, *University College London.* Paul Kirsch, Raj Jammy, *SEMATECH.*

18:20 **Extracting Accurate Position and Energy Level of Oxide Trap Generating Random Telegraph Noise(RTN) in Recessed Channel MOSFET's**
Sunyoung Park, Sanghoon Lee, Yeonsung Kang, Byung-Gook Park, Jong-Ho Lee, *Seoul National University.* Jooyoung Lee, Gyoyoung Jin, *Samsung Electronics Co., Ltd.* Hyungcheol Shin, *Seoul National University.*

WEDNESDAY SEPTEMBER 15

Tunneling FET devices
(Lecture)

Session Code:	B6L-C
Location:	Room E
Date & Time:	Wednesday September 15, 2010 (17:20 - 18:40)
Chair(s):	Jean-Pierre Colinge, *Tyndall National Institute, Ireland* Stephane Monfray, *STMicroelectronics, France*

17:20 **SOI TFETs: Suppression of Ambipolar Leakage and Low-Frequency Noise Behavior**
Jing Wan, *IMEP-INPG/Minatec.* Cyrille Le Royer, *CEA-LETI Minatec.* Alexander Zaslavsky, *Brown University.* Sorin Cristoloveanu, *IMEP-INPG/ Minatec.*

17:40 **A Simulation-Based Study of Sensitivity to Parameter Fluctuations of Silicon Tunnel FETs**
Kathy Boucart, *EPFL Ecole Polytechnique Federale de Lausanne.* Walter Riess, *IBM Research - Zurich.* Adrian M. Ionescu, *EPFL Ecole Polytechnique Federale de Lausanne.*

18:00 **Impact of Electron Velocity on the I_{ON} of n-TFETs**
Hasanali Virani, *Indian Institute of Technology, Bombay.* David Esseni, *University of Udine.* Anil Kottantharayil, *Indian Institute of Technology.*

18:20 **Abrupt Switch Based on Internally Combined Band-to-Band and Barrier Tunneling Mechanisms**
Livio Lattanzio, Luca De Michielis, EPFL *Ecole Polytechnique Federale de Lausanne.* Arnab Biswas, *Vellore Institute of Technology/EPFL.* Adrian M. Ionescu, *EPFL Ecole Polytechnique Federale de Lausanne.*

THURSDAY SEPTEMBER 16

Nanowire Transistors
(Lecture)

Session Code:	C3L-B
Location:	Room B
Date & Time:	Thursday September 16, 2010 (11:20 - 13:00)
Chair(s):	Emmanuel Dubois, IEMN, *France* Thomas Ernst, *CEA-LETI, France*

11:20 **Junctionless Nanowire Transistor (JNT): Properties and Design Guidelines**
Abhinav Kranti, Ran Yan, Chi-Woo Lee, Isabelle Ferain, Ran Yu, Nima Dehdashti Akhavan, Pedram Razavi, Jean-Pierre Colinge, *Tyndall National Institute.*

11:40 **Gate Semi-Around Si Nanowire FET Fabricated by Conventional CMOS Process with Very High Drivability**
Soshi Sato, Yeonghun Lee, Kuniyuki Kakushima, Parhat Ahmet, *Tokyo Institute of Technology.* Kenji Ohmori, *Waseda University.* Kenji Natori, *Tokyo Institute of Technology.* Keisaku Yamada, *Waseda University.* Hiroshi Iwai, *Tokyo Institute of Technology.*

12:00 **Dopant-Independent and Voltage-Selectable Silicon-Nanowire-CMOS Technology for Reconfigurable Logic Applications**
Frank Wessely, Tillmann Krauss, Udo Schwalke, *Darmstadt University of Technology.*

12:20 **3D Source/Drain Doping Optimization in Multi-Channel MOSFET**
Kiichi Tachi, *CEA-LETI, Minatec/IMEP-LAHC/ Tokyo Institute of Technology.* Nathalie Vulliet, *STMicroelectronics.* Sylvain Barraud, *CEA-LETI, Minatec*. Bernard Guillaumot, *STMicroelectronics.* Virginie Maffini-Alvaro, Christian Vizioz, *CEA-LETI, Minatec*. Christian Arvet, Y. Campidelli, *STMicroelectronics. P. Gautier,* Jean-Michel Hartmann, *CEA-LETI, Minatec*. Thomas Skotnicki, *STMicroelectronics.* Sorin Cristoloveanu, *IIMEP-LAHC/ INPG-MINATEC.* Hiroshi Iwai, *Tokyo Institute of Technology.* Olivier Faynot, Thomas Ernst, *CEA-LETI, Minatec*.

12:40 **Hole Mobilities and Electrical Characteristics of Omega-Gated Silicon Nanowire Array FETs with {110} - and {100} - Channel Orientation**
Stefan Habicht, Sebastian Feste, Qing Tai Zhao, Siegfried Mantl, *Forschungszentrum Juelich.*

Device steep slope and leakage
(Lecture)

Session Code: C3L-C

Location: Room E

Date & Time: Thursday September 16, 2010
(11:20 - 12:40)

Chair(s): David Esseni,
Unversity of Udine, Italy
Tibor Grasser,
TU-Wien, Austria

11:20 **Breaching the kT/q Limit with Dopant Segregated Schottky Barrier Resonant Tunneling MOSFETs: a Computationnal Study**
Aryan Afzalian, Denis Flandre, *UCL Université Catholique de Louvain.*

11:40 **Steep-Slope Nanowire FET with a Superlattice in the Source Extension**
Elena Gnani, Susanna Reggiani, Antonio Gnudi, Giorgio Baccarani, *University of Bologna.*

12:00 **Modeling Impact of Electric Field and Strain on the Leakage of Embedded SiGe Source/Drain Junctions**
Abraham Luque Rodríguez, Juan Antonio Jiménez Tejada, Salvador Rodríguez Bolívar, *University of Granada.* Mireia Bargallo González, *IMEC/KU Leuven.* Geert Eneman, *IMEC/KU Leuven*/*FWO-Vlaanderen.* Cor Claeys, *IMEC/KU Leuven.* Eddy Simoen*, IMEC.*

12:20 **Modeling Temperature Dependency (6 - 400K) of the Leakage Current Through the SiO_2/High-K Stacks**
Luca Vandelli, Andrea Padovani, Luca Larcher, *Universitá di Modena e Reggio Emilia.* Richard Southwick, Bill Knowlton, *Boise State University.* Gennadi Bersuker, *SEMATECH*

THURSDAY SEPTEMBER 16

Advanced Memories
(Lecture)

Session Code: C3L-D

Location: Room D

Date & Time: Thursday September 16, 2010 (11:20 - 13:00)

Chair(s): Luc Haspeslagh, *IMEC*, *Belgium*
Fernanda Irrera, *University "La Sapienza" of Roma, Italy*

11:20 **Oxide-Based RRAM: Physical Based Retention Projection**
Bin Gao, Jinfeng Kang, Haowei Zhang, Bing Sun, Bing Chen, Lifeng Liu, Xiaoyan Liu, Ruqi Han, Yangyuan Wang, *Institute of Microelectronics, Peking University.* Zheng Fang, Hongyu Yu, *Nanyang Technological University.* Bin Yu, *State University of New York, Albany.* Dim-Lee Kwong, *Institute of Microelectronics, A STAR Singapore.*

11:40 **A Stochastic Model of Bipolar Resistive Switching in Metal-Oxide-Based Memory**
Alexander Makarov, Viktor Sverdlov, Siegfried Selberherr, *Institute for Microelectronics, TU Wien.*

12:00 **Dependence of the Switching Characteristics of Resistance Random Access Memory on the Type of Transition Metal Oxide**
Wan Gee Kim, Min Gyu Sung, Sook Joo Kim, Ja Yong Kim, Ji Won Moon, Sung Joon Yoon, Jung Nam Kim, Byung Gu Gyun, Taeh Wan Kim, Chi Ho Kim, Jun Young Byun, Won Kim, Te One Youn, Jong Hee Yoo, Jang Won Oh, Ho Joung Kim, Moon Sig Joo, Jae Sung Roh, Sung Ki Park, *Hynix semiconductor Inc.*

12:20 **A 3d Stackable Carbon Nanotube-Based Nonvolatile Memory (NRAM)**
Sohrab Kianian, Glen Rosendale, Monte Manning, Darlene Hamilton, Xue Ming Henry Huang, Karl Robinson, Young Weon Kim, Thomas Rueckes, *Nantero Inc.*

12:40 **Experimental and Simulation Study of the Program Efficiency of HfO_2 Based Charge Trapping. Memories**
Sabina Spiga, Gabriele Congedo, Ugo Russo, Alessio Lamperti, Olivier Salicio, *Laboratorio MDM, IMM-CNR.* Francesco Driussi, Elisa Vianello, *University of Udine.*

THURSDAY SEPTEMBER 16

Channel and Gate Stack Engineering
(Lecture)

Session Code: C4L-B

Location: Room B

Date & Time: Thursday September 16, 2010
(14:50 - 15:50)

Chair(s): Andrés Godoy,
University of Granada, Spain
Thomas Skotnicki,
STMicroelectronics, France

14:50 **Carrier Transport Characteristics of Strained N-MOSFET Featuring Channel Proximate Silicon-Carbon Source/Drain Stressors for Performance Boost**
Shao-Ming Koh, Peng Zhang, Shu-Feng Ren, *National University of Singapore.* Chee-Mang Ng, *Global Foundries Singapore Pte. Ltd.* Ganesh S. Samudra, Yee-Chia Yeo, *National University of Singapore.*

15:10 **Fluorinated CMOS HfO_2 for High Performance (HP) and Low Stand-by Power (LSTP) Application by Pre- and Post-CF_4 Plasma Passivation**
Woei-Cherng Wu, *National Chiao Tung University.* Chao-Sung Lai, Huai-Hsien Chiu, Jer-Chyi Wang, Pai-Chi Chou, *Chang Gung University.* Tien-Sheng Chao, *National Chiao Tung University.*

15:30 **Origins of Universal Mobility Violation in SOI MOSFETs**
Noel Rodríguez, *University of Granada.* Sorin Cristoloveanu, *IMEP-INPG-Minatec.* Francisco Gámiz, *University of Granada.*

THURSDAY SEPTEMBER 16

Simulation of III/V devices
(Lecture)

Session Code:	C4L-C
Location:	Room E
Date & Time:	Thursday September 16, 2010 (14:50 - 15:50)
Chair(s):	Wim Schoenmaker, *Magwel, Belgium*

14:50 **Optimization of III-V FETs Architecture for High Frequency and Low Consumption Applications**
Ming Shi, Jérôme Saint-Martin, Arnaud Bournel, Philippe Dollfus, *University of Paris.*

15:10 **Vertical Design of InN Field Effect Transistors**
Ralf Granzner, *TU Technische Universitaet Ilmenau.* Vladimir Polyakov, *Fraunhofer IAF Institute for Applied Solid State Physics.* Mario Kittler, Frank Schwierz, *TU Ilmenau.*

15:30 **A Continuous Physics-Based Electrothermal Compact Model for the Study of Non-Linearities in III-V HEMTs**
Toufik Sadi, Frank Schwierz, *TU Technische Universitaet Ilmenau.*

Charge Trap NAND Flash
(Lecture)

Session Code: C4L-D

Location: Room D

Date & Time: Thursday September 16, 2010
(14:50 - 15:50)

Chair(s): Giorgio Baccarani,
University of Bologna, Italy

14:50 **Investigation of Rare-Earth Aluminates As Alternative Trapping Materials in Flash Memories**
Antonio Cacciato, Amit Suhane, Olivier Richard, Antonio Arreghini, Christoph Adelmann, Johan Swerts, Aude Rothschild, Geert Van Den Bosch, Hugo Bender, Malgorzata Jurczak, Ingrid Debusschere, Jorge Kittl, Jan Van Houdt, *IMEC.*

15:10 **Optimization of the Crystallization Phase of Rare-Earth Aluminates for Blocking Dielectric Application in TANOS Type Flash Memories**
Laurent Breuil, Christoph Adelmann, Geert Van Den Bosch, Antonio Cacciato, Mohammed B. Zahid, María Toledano-Luque, Amit Suhane, Antonio Arreghini, Robin Degraeve, S. Van Elshocht, Ingrid Debusschere, Jorge Kittl, Margorzata Jurczak, Jan Van Houdt, *IMEC.*

15:30 **Investigation of the ISPP Dynamics and of the Programming Efficiency of Charge-Trap Memories**
Alessandro Maconi, Christian Monzio Compagnoni, Salvatore M. Amoroso, Evelyne Mascellino, Michele Ghidotti, Giorgio Padovini, Alessandro S. Spinelli, Andrea L. Lacaita, *Politecnico di Milano.*
Aurelio Mauri, Gabriella Ghidini, Nadia Galbiati, Alessandro Sebastiani, Claudia Scozzari, Eugenio Greco, Elisa Camozzi, Paolo Tessariol, *Numonyx R&D.*

THURSDAY SEPTEMBER 16

Analytical/compact models
(Lecture)

Session Code: C6L-B

Location: Room B

Date & Time: Thursday September 16, 2010 (17:20 - 18:40)

Chair(s): Ray Hueting, *University of Twente, The Netherlands*
Benjamín Iñiguez, *Universitat Rovira i Virgili, Spain*

17:20 **3D Analytical Modelling of Subthreshold Characteristics in Pi-Gate FinFET Transistors**
Romain Ritzenthaler, Francois Lime, *Rovira i Virgili University*. Olivier Faynot, *CEA-Leti Minatec.* Sorin Cristoloveanu, *IMEP LAHC INPG Minatec* Benjamín Iñiguez, *Universitat Rovira i Virgili.*

17:40 **A Compact Model for Double Gate Carbon Nanotube FET**
Sebastien Fregonese, Cristell Maneux, Thomas Zimmer, *Bordeaux University.*

18:00 **Modeling of Partial-Reset Dynamics in Phase Change Memories**
Stefania Braga, Alessandro Sanasi, Alessandro Cabrini, Guido Torelli, *University of Pavia.*

18:20 **On the Modelling and Optimisation of a Novel Schottky Based Silicon Rectifier**
Tom van Hemert, Ray Hueting, Bijoy Rajasekharan, Cora Salm, Jurriaan Schmitz, *University of Twente.*

Electromechanical Devices
(Lecture)

Session Code: C6L-C

Location: Room E

Date & Time: Thursday September 16, 2010 (17:20 - 18:40)

Chair(s): Eugenio Cantatore, *TU/e, Eindhoven. Netherlands*
Harold Gamble, *Queen´s University Belfast, Uk*

17:20 **CMOS-MEMS Free-Free Beam Resonators**
Joan Lluis Lopez, Eloi Marigo, Joan Giner, Jose Luis Muñoz-Gamarra, Francesc Torres, Arantxa Uranga, Nuria Barniol, *UAB Universitat Autònoma de Barcelona.*

17:40 **Electro-Thermal Analysis of RF MEM Capacitive Switches for High-Power Applications**
Francesco Solazzi, Cristiano Palego, Subrata Halder, James C. M. Hwang, *Lehigh University.* Alessandro Faes, Viviana Mulloni, Benno Margesin, *FBK Fondazione Bruno Kessler.* Paola Farinelli, Roberto Sorrentino, *RF Microtech.*

18:00 **Active NEM Filters for Communications Applications Based on Vibrating Body Transistors**
Andrea Lovera, Sebastian Bartsch, Daniel Grogg, Suat Ayoz, *EPFL Ecole Polytechnique Federale de Lausanne.* Risto Kaunisto, *Nokia.* Adrian Mihai Ionescu, *EPFL Ecole Polytechnique Federale de Lausanne.*

18:20 **Piezoresistivity and Electrical Properties of Poly-SiGe Deposited at CMOS-Compatible Temperatures**
Pilar González, *IMEC/KU Leuve.* Luc Haspeslagh, Simone Severi, *IMEC.* Kristin De Meyer, *IMEC/KU Leuve.* Ann Witvrouw, *IMEC.*

FRIDAY, SEPTEMBER 17TH, 2010

SILICON ON INSULATOR: MATERIALS TO CIRCUIT DESIGN

Dr. Francis Balestra, *Grenoble INP*, Raphael Clerc, *IMEP-MINATEC, Grenoble*.

Abstract

This Workshop is supported by the SINANO Institute and by the European Network of Excellence NANOSIL funded by the European Commission for the 7th Framework Programme

Research in Nanoelectronics today not only consists in pushing further the tremendous scaling of integrated circuits. It is also about introducing additional functionalities such as micro/nanosystem, RF, analog, biochips ... with more conventional logic or memory circuits. In addition, new technologies (such as for instance graphene or nanowire electronics) are also expected to emerge from the area of Nanosciences and Nanotechnologies, possibly leading to major breakthroughs for many applications.

These main trends, referred as “More Moore”, “More Than Moore” and “Beyond CMOS”, are usually presented as three distinct fields. But is it so simple? In Physics, Technology and Design: what are in fact the connections between these three domains? What are the synergies needed between the various aspects of Nanoelectronics? Is there a convergence between future research topics and platforms in these areas?

Several outstanding speakers, coming both from industry and academia, on the basis of examples taken from their own expertise and vision, will address this very important issue for future Nanoelectronic systems.

Agenda

8:45–9:00
Welcome and Opening

9:00–9:30
III-V high mobility materials in advanced CMOS
Thomas Skotnicki, STMicroelectronics, France

9:30–10:00
CMOS, CMORE, and what to use it for
Sywert Brongersma, IMEC, Belgium

10:00–10:30 Coffee Break

10:30–11:00
When More Moore meets More than Moore and Beyond CMOS
Enrico Sangiorgi, IU.NET, Italy

11:00–11:30
Nanowires in the Beyond CMOS and More than Moore perspectives: Electromechanical properties
Mireille Mouis, IMEP-LAHC, France
11:30–12:00
Scaling Challenges for complex SOC products
Rainer Kress, Infineon Technologies, Germany
12:00–13:00 Lunch
13:00–13:30
Tunnel Field Effect Transitors based on grown Nanowires
Heike Riel, IBM Research, Switzerland
13:30–14:00
Synergies and differences between More Moore, More than Moore and Beyond CMOS
Michel Brillouet, CEA LETI, France
14:00–14:30
Novel Materials, a source of innovation and performance gain
Siegfried Mantl, Forschungszentrum Juliech, Germany
14:30–15:00
Diversification of Moore's law and its advanced technologies
Jan Hoentschel, Global Foundries, Germany
15:00–15:30
Junctionless nanowire transistor: an example of the convergence between More Moore and Beyond CMOS
Jean Pierre Colinge, Tyndall, Ireland

NEMSIC: Nano-Electro-Mechanical Devices for Integrated Sensing and Switching.

Dr. Tsamados, A.M. Ionescu, *Ecole Polytechnique Fédérale de Lausanne, Switzerland.* H. Mizuta, *University of Southampton, UK.*

Abstract
This Workshop is supported by the NEMSIC FP7 STREP funded by the European Commission, see:
http://www.nemsic.org/
To detect a carcinogen, a pharmaceutically active compound or toxic gases in the environment within seconds thanks to a handheld device on an electronic chip: such a revolution that may be made possible through the integration of so-called NEMS, miniaturized electromechanical structures in which at least one dimension is of nanometre scale.
The devices targeted in the framework of the FP7 STREP project NEMSIC at the heart of the "intelligent sensor system" are suspended nanowires excited to vibrate at their res-

onance frequencies. The wire is chemically or biologically functionalized to make it selective for target molecules like carcinogens. Binding of target molecules leads to an increase in the mass of the wire which in turn will change its resonance frequency and vibrate at a lower frequency (think of a violin: the thicker the string the lower the tone).
The workshop will include state-of-the-art progress reports on NEMS devices and applications, with invited keynotes from USA and Japan and the detailed technical reports on the status of NEMSIC research.

Agenda

8:45–9:00
Opening and short overview of NEMSIC project
A.M. Ionescu, Ecole Polytechnique Fédérale de Lausanne, Switzerland

9:00–9:30
Keynote 1: Hybrid NEMS Resonators
S. Bhave, Cornell University, USA

9:30–10:00
Suspended silicon nanowire sensing based on conductance and mass detection
Y. Tsuchiya, F. Arab Hassani, M. A. Ghiass, Z. Moktadir, and H. Mizuta
School of Electronics and Computer Sc., University of Southampton, UK
S. Armini, M. Carli, A. Maestre Caro, V. Cherman
IMEC, Belgium

10:00–10:30 Coffee Break

10:30–11:00
Towards integration of Nanowires with FDSOI transistors: from design to technology
E. Ollier, CEA-LETI, France

11:00–11:30
Resonant body FinFETs
D. Grogg, S. Bartch, D. Tsamados, A.M. Ionescu
Ecole Polytechnique Fédérale de Lausanne, Switzerland

11:30 – 12:00
Circuit design for NEMS/MEMS resonator gas sensors
V. Petrescu, IMEC, The Netherlands

12:00–13:00 Lunch

13:00–13:30
Keynote 2: NEMS Scaled Silicon NEM hybric devices
Shunri Oda, Tokyo Institute of Technology, Japan.

13:30–13:50
Novel concepts for NO2 detection by differential resonant nanosensing
B. Serban, C. Cobianu
ACS Sensors &Wireless Laboratory Bucharest, Honeywell Romania SRL

13:50–14:10
NEMS in biological applications
D. Bertrand
Dpt of Neuroscience, Medical Faculty & HiQscreen, Switzerland

14:10–14:30
Modeling and simulation tools for the development of nanoscale suspended-gate MOSFETs (NEMFET) and Vibrating-body FETs (VBFET) for bulk-Si and SOI technologies
D. Tsamados
Ecole Polytechnique Fédérale de Lausanne, Switzerland.

14:30–14:50 Coffee Break

14:50-15:20
Keynote 3: TBD
A. B. Smit
NEUROCYPRES Consortium

15:20-15:40
Nanoscale Silicon Nanowires Surface Functionalization and Characterization for Sensing Applications
S. Armini, M. Carli, V. Cherman, A. Maestre Caro, J. Moonens, P. Neutens,
IMEC, Kapeldreef 75, B-3001 Heverlee, Leuven, Belgium
J. Ogi, S. Oda,
Tokyo Institute of Technology, Tokyo, Japan
Y. Tsuchiya, H. Mizuta
University of Southampton, SO17 1BJ, Southampton, United Kingdom

15:40–16:00
Suspended Gate -Field Effect Transistor (SG-FET) Based Advanced Power Management in CMOS ICs
M. Enachescu, S. Cotofana
Computer Engineering Laboratory, Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, the Netherlands.

16:00–16:20
New developments in carbon nanotubes synthesis for NEMs application
A. Magrez
Ecole Polytechnique Fédérale de Lausanne, Switzerland

16:20–16:40
CNT NEM switches for RF applications
D. Aquaviva
Ecole Polytechnique Fédérale de Lausanne, Switzerland
16:40 Closing

MOS-AK/GSA WORKSHOP: "FRONTIERS OF THE COMPACT MODELING FOR ADVANCED ANALOG/ RF APPLICATIONS".

Dr. Wladek Grabinski, *GMC Suisse*.

HiTech forum to discuss the frontiers of electron device modeling with emphasis on simulation-aware models.
MOS-AK/GSA Meetings are organized with aims to strengthen a network and discussion forum among experts in the field, enhance open platform for information exchange related to compact/Spice modeling and Verilog-A standardization, bring people in the compact modeling field together, as well as obtain feedback from technology developers, circuit designers, and CAD tool vendors. The topics cover all important aspects of compact model development, implementation, deployment and standardization within the main theme - frontiers of the compact modeling for nm-scale MEMS designs and CMOS/SOI circuit simulation.

Synopsis

The specific workshop goal will be to classify the most important directions for the future development of the electron device models, not limiting the discussion to compact models, but including physical, analytical and numerical models, to clearly identify areas that need further research and possible contact points between the different modeling domains. This workshop is designed for device process engineers (CMOS, SOI, BiCMOS, SiGe) who are interested in device modeling; ICs designers (RF/Analog/Mixed-Signal/SoC) and those starting in that area as well as device characterization, modeling and parameter extraction engineers. The content will be beneficial for anyone who needs to learn what is really behind the IC simulation in modern device models.

Topics

- Compact Modeling (CM) of the electron devices
- Verilog-A language for CM standardization
- New CM techniques and extraction software
- CM of passive, active, sensors and actuators
- Emerging Devices, CMOS and SOI-based memory cells

- Microwave, RF device modeling, high voltage device modeling
- Nanoscale CMOS devices and circuits
- Technology R&D, DFY, DFT and IC Designs
- Foundry/Fabless Interface Strategies

ITRS WORKSHOP ON EMERGING SPIN AND CARBON BASED EMERGING LOGIC DEVICES

Dr. Bourianoff George, *Intel Corp*, Dr. James Hutchby, *Semiconductor Research Corporation,* A.M. Ionescu, *Ecole Polytechnique Fédérale de Lausanne*.

Background

In September 2008, the ITRS Technology Working Group on Emerging Research Logic Devices organized a focused workshop in Tsukuba, Japan (September 2008) relating to carbon-based nanoelectronic and spin transfer torque logic devices in preparation for the 2009 rewrite of the ITRS. That workshop, mapped out some key research needs and technology challenges associated with those two technologies. In the intervening two years, a great deal of progress has been made in both technologies and it is now time to organize a similar workshop in order to expand and update the information that will be included in the 2011 rewrite of the ITRS.

Objectives

The 2010 ITRS/ERD workshop, co-sponsored by NSF, will have several objectives in keeping with the established two year rewrite cycle for the ITRS roadmap document. The primary objective of this workshop is to gather material on selected research areas in order to have current information for the 2011 chapter rewrite. This year the research areas are spin based logic elements and graphene based logic. The second objective is to hold a brief business meeting to review the structure of the chapter relating to technology entries, and the primary table structure for the rewritten chapter. Due to the limited time available, the business meeting will be limited to reviewing the decisions made at the summer ERD meeting in San Francisco and soliciting input.

Abstract

The workshop will be based on the special focused workshop described above plus two additional annual ERD workshops, one in April 2008 in Koenigswinter, Germany and the other in San Francisco (July 2008). The July, 2008, workshop was

organized with the express objective of evaluating the relative maturity of the entire set of emerging logic technologies that had been tracked by the ITRS ERD since 2001. The conclusion of this workshop was that none of the ERD tracked technologies was likely to replace scaled CMOS as the dominant information processing technology, but that some technologies had the potential to be superior to scaled silicon in certain specialized applications. Among these technologies, carbon-based nanoelectronics was judged to be the most mature and as such could benefit most from additional research funding. It was also explicitly concluded that all of the technology entries should continue to receive additional funding because it would premature to eliminate any of the options completely. A similar assessment of emerging memory technologies, held in April 2010, concluded that spin transfer torque MRAM and a "Redox" resistive memory were good candidates for accelerated research and development – thus ERD's continuing focus on spin nanodevices.

Agenda

8:00-8:15 Welcome and Introduction

8:15–12:15

Evaluate status, progress, and research needs for spin based logic elements

Moderator: G. Bourianoff

- Overview of DARPA Spin Logic program, Dev Shenoy
- MQCA, Jeff Bokor, Berkeley
- Spin torque logic gates
- All spin logic, Behtash Behin-Aein, Purdue
- Magnetic FPGAs, memory in logi, c Takahiro Hanyu, Tohoku University
- TIMARIS: Linear Dynamic Deposition technology for production of Spintronic Devices, W. Maass, Singulus
- Wrap-up discussion (30min)

12:15-13:15 Lunch

13:15-17:15

Evaluate status, progress, and research needs for graphene logic devices

Moderator: (tbd)

- Graphene logic devices, P. Kim, Columbia
- RF and Analog Graphene based FETs, C. Sung, IBM
- GRAND perspectives of graphen electronics, H. Kurz, AMO
- Speaker from Japan
- CEA, S. Roche
- Wrap-up discussion (30min)

17:15-17:30 Break

17:30-18:30
Business meeting
General information
Presentations at the workshop is by invitation only. Attendance at the workshop is open to all interested parties who wish to participate.

For further information about these workshops, please visit the webpage of the conference at http://www.essderc2010.org/essdercWor.html

ESSDERC FRINGE

The ESSDERC Fringe Poster will be held in the Exhibition Area near the "Atrio III" (please refer to the map available in this program). The posters will be introduced by their authors during three different Fringe Poster Briefing Sessions on Tuesday 14th (please refer to the timetable). Poster will be then displayed from Tuesday 14th to Thursday 16th. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange a discussion with any of the presenters.

P1 Two Dimensional Si-MOSFET Numerical Model for Heat Conduction Analysis
H. Djelt et al., Laboratoire STIC, Algeria

P2 Performance Estimation of Carbon Nanowall-based Field Effect Transistor by 3D Simulation Study
A. Malinowski et al., Nagoya University Nagoya, Japan

P3 Embedded DRAM Future Trends: from 1T1C eDRAM to a 1T-Bulk gen2 Capacitor-less DRAM
R. Pulicani et al., STMicroelectronics, France

P4 SOI Field-Effect-Diodes for Memory Cell Design
Y. Yang et al., George Mason University, USA

P5 Si on SiC, a novel platform for MOS power devices
A. Pérez-Tomás et al., University of Warwick, IMB-CNM-CSIC, Spain

P6 Improvement of Cell Vth Distribution with Nitrogen-Doped Polysilicon for Floating Gate
K.-C. Joo et al., Hynix Semiconductor Inc., Korea

P7 Electrical Characteristics of Lateral Modified Schottky Barrier P+-N Junctions on SOI Substrate
B.-Y. Tsui et al., Hsinchu University, Republic of China

P8 2D Analytical Calculation of the Tunneling Current in Lightly Doped Schottky Barrier Double-Gate MOSFET
M. Schwarz et al., University of Applied Sciences Giessen-Friedberg, Germany

P9 Characterization and Packaging of Grating-Coupled Silicon-on-Insulator (SOI) Photonic Devices
B. Snyder et al., Tyndall National Institute, Ireland

P10 High-resistivity Czochralski-silicon using Deep Level Dopant Compensation
A. Abuelgasim et al., University of Southampton, UK

P11 Thermal Behavior modeling of NLDMOS-SOI devices using Distributed Thermal Network
S. Hniki et al., STMicroelectronics, France

P12 A Simple Model for Current-Voltage Characteristics of Graphene Based Devices
O. Moldovan et al., UAB, Spain

P13 Low-Field Resistance Drift in Partial-SET States in Phase Change Memories
S. Braga et al., University of Pavia, Italy

P14 Surface potential amplification model of the negative capacitance FET
D. Jiménez et al., University of Granada, Spain

P15 Silicon Nanowire Based MESFET Fabricated Using CMOS Technology on SOI wafer
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