ESSDERC Fringe Posters

The ESSDERC Fringe Poster will be held in the Exhibition Area near the "Atrio III" (please refer to the map available in this program). The posters will be introduced by their authors during three different Fringe Poster Briefing Sessions on Tuesday 14th (please refer to the timetable). Poster will be then displayed from Tuesday 14th to Thursday 16th. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange a discussion with any of the presenters.

P1 Two Dimensional Si-MOSFET Numerical Model for Heat Conduction Analysis
H. Djelt et al., Laboratoire STIC, Algeria

P2 Performance Estimation of Carbon Nanowall-based Field Effect Transistor by 3D Simulation Study
A. Malinowski et al., Nagoya University Nagoya, Japan

P3 Embedded DRAM Future Trends: from 1T1C eDRAM to a 1T-Bulk gen2 Capacitor-less DRAM
R. Pulicani et al., STMicroelectronics, France

P4 SOI Field-Effect-Diodes for Memory Cell Design
Y. Yang et al., George Mason University, USA

P5 Si on SiC, a novel platform for MOS power devices
A. Pérez-Tomás et al., University of Warwick, IMB-CNM-CSIC, Spain

P6 Improvement of Cell Vth Distribution with Nitrogen-Doped Polysilicon for Floating Gate
K.-C. Joo et al., Hynix Semiconductor Inc., Korea

P7 Electrical Characteristics of Lateral Modified Schottky Barrier P+-N Junctions on SOI Substrate
B.-Y. Tsui et al., Hsinchu University, Republic of China

P8 2D Analytical Calculation of the Tunneling Current in Lightly Doped Schottky Barrier Double-Gate MOSFET
M. Schwarz et al., University of Applied Sciences Giessen-Friedberg, Germany

P9 Characterization and Packaging of Grating-Coupled Silicon-on-Insulator (SOI) Photonic Devices
B. Snyder et al., Tyndall National Institute, Ireland

P10 High-resistivity Czochralski-silicon using Deep Level Dopant Compensation
A. Abuelgasim et al., University of Southampton, UK

P11 Thermal Behavior modeling of NLDMOS-SOI devices using Distributed Thermal Network
S. Hniki et al., STMicroelectronics, France

P12 A Simple Model for Current-Voltage Characteristics of Graphene Based Devices
O. Moldovan et al., UAB, Spain

P13 Low-Field Resistance Drift in Partial-SET States in Phase Change Memories
S. Braga et al., University of Pavia, Italy

P14 Surface potential amplification model of the negative capacitance FET
D. Jiménez et al., University of Granada, Spain

P15 Silicon Nanowire Based MESFET Fabricated Using CMOS Technology on SOI wafer
Y. Sun et al., Nanyang Technological University, Singapore

P16 An Alternative Characterization Method of pFET Subthreshold Slope under NBTI Stress
R. Fernández et al., UPC, Spain

P17 Low-Temperature Integration of Nanoparticulate Zinc Oxide FETs on Glass Substrate
F. Assion et al., University of Paderborn, Germany

P18 Hydrodynamic Models for GaN-Based HEMTs
S. Vitanov et al., Technische Universitaet Wien, Austria

P19 Deep Levels Impact on System performances
M. Jaafar-Belhouji, University of Limoges, France

P20 Interfacing to Large Area CVD Monolayer Graphene: Devices and Analysis
O. M. Nayfeh et al., United States Army Research Laboratory, USA

P21 Transient Simulations of the Lateral Drift-Field Photodetector for 0.35µm CMOS Imaging Sensors
R. Mahdi et al., Fraunhofer Institut IMS, Germany

P22 Design and Analysis of Double Spin Qubits Integrated on Ultra-thin Silicon-on-insulator
F. M. Alkhalil et al., University of Southampton, UK

P23 Non-Linearity of Transconductance and Source-Gate Resistance of HEMTs
S. Vitanov et al., Technische Universitaet Wien, Austria