ESSCIRC Fringe Posters

The ESSCIRC Fringe Poster will be held in the Exhibition Area near the "Atrio III" (please refer to the map available in this program). The posters will be introduced by their authors during three different Fringe Poster Briefing Sessions on Tuesday 14th (please refer to the timetable). Poster will be then displayed from Tuesday 14th to Thursday 16th. Presenters will also be on hand to discuss their posters outside this timeslot by prior arrangement. Please come to the registration desk to arrange a discussion with any of the presenters.

P1 Low Side Switch Short Circuit Protection Optimized for High Current Inrush Loads

A. Danchiv, D. Manta, M. Hulub (*Infineon Technologies Romania*)

P2 Behavioral Modeling in Automotive Industry – CAN Transceiver

C. Dolea, C. Ivu (*Infineon Technologies, Romania*), M.-M. Hell (*Infineon Technologies, Germany*)

P3 A 32x32 pixels vision sensor for Selective Change Driven readout strategy

P. Zuccarello, Fernando Pardo (*Department of Informatics Universitat de Valencia, Spain*), A. de la Plaza (*Universidad de Buenos Aires, Argentina*), J. A. Boluda (*Department of Informatics Universitat de Valencia, Spain*)

P4 A low power multi-bit phase sampling circuit for VCO based ADCs

M. Voelker (*Fraunhofer Institute for Integrated Circuits IIS, Germany*)

P5 Hybrid SAR-Slope ADC for CMOS Image Sensors

H. Neubauer (*Fraunhofer Institute for Integrated Circuits IIS, Germany*)

P6 A Radio Frequency Receiver IC for Digital Video Broadcasting - Satellite services to Handhelds

H. García-Vázquez et al., Universidad de las Palmas de Gran Canaria, Spain

P7 An Improved High-Speed High-Resolution Comparator to be Used in Pipelined Analog-to-Digital Converters

D. Yang et al., Microelectronics Technology Institute Beijing, Republic of China

P8 Pseudo H-Bridge Current Cell DAC for High Speed Continuous-Time ΣΔ ADCs

J. Segundo et al., University of Valladolid, Spain

P9 Low power 2.4 GHz quadrature generators for Bluetooth LE

J. Masuch et al., IMSE-CNM-CSIC and University of Seville, Spain

P10 A Parallel Continuous-Time ΣΔ ADC for OFDM UWB Receivers in 130 nm CMOS Technology

J. Segundo et al., University of Valladolid, Spain

P11 Design of Injection-Locked Frequency Divider in 65 nm CMOS Technology for mm-W applications

D. Brandano et al., UPC, Spain

P12 Analog Circuit Synthesis: EDA'S Nightmare and Designer's Dream

A. Momin, TES Electronic Solutions GmbH, Germany

P13 Sensitivity Analysis Based Analytical Evaluation of Aging Degradation in Linear Circuits

S. More et al., Technische Universität München, Germany

P14 A Low-voltage Current-mode Log-domain Integrator using MOS in Sub-threshold
L. Ramezani, Islamic Azad University, Iran

P15 Synaptic Weight Storage and Update In Silicon Neurons
A. Smith, University of Liverpool, UK

P16 A Signal Processing System for Recognition of Acoustic Emergency Signals
M. Mielke, University of Siegen, Germany

P17 12.5 Gbit/s Configurable Threefold 2:1 MUX and 1:2 DEMUX Chips in 130 nm CMOS Technology
H. Huang et al., University of Stuttgart, Germany

P18 Dual-Mode Switched-Capacitor DC-DC Converter for Subthreshold Processors with Deep Sleep Mode
J. De Vos et al., Université Catholique de Louvain, Belgium

P19 In-Situ Monitoring to Adapt for PVT-Variations
M. Wirnshofer et al., Technische Universitat Munchen, Germany

P20 S-Parameter Measurement-Based Modeling Methodology for On-Chip Interconnects used in High Frequency Systems
O. González-Díaz et at., INAOE, Mexico

P21 A FPP-Oriented Tone Mapping Technique for High Dynamic Range Imagers using Temporal and Final Exposure Measurements
S. Vargas-Sierra et al., IMSE-CNM-CSIC and University of Seville, Spain