ITRS workshop on Emerging Spin and Carbon Based Emerging Logic Devices

September 17, 2010, Seville, Spain

Background: In September 2008, the ITRS Technology Working Group on Emerging Research Logic Devices organized a focused workshop in Tsukuba, Japan (September 2008) relating to carbon-based nanoelectronic and spin transfer torque logic devices in preparation for the 2009 rewrite of the ITRS. That workshop, mapped out some key research needs and technology challenges associated with those two technologies. In the intervening two years, a great deal of progress has been made in both technologies and it is now time to organize a similar workshop in order to expand and update the information that will be included in the 2011 rewrite of the ITRS.

Objectives: The 2010 ITRS/ERD workshop, co-sponsored by NSF, will have several objectives in keeping with the established two year rewrite cycle for the ITRS roadmap document. The primary objective of this workshop is to gather material on selected research areas in order to have current information for the 2011 chapter rewrite. This year the research areas are spin based logic elements and graphene based logic. The second objective is to hold a brief business meeting to review the structure of the chapter relating to technology entries, and the primary table structure for the rewritten chapter. Due to the limited time available, the business meeting will be limited to reviewing the decisions made at the summer ERD meeting in San Francisco and soliciting input.

Workshop: The workshop will be based on the special focused workshop described above plus two additional annual ERD workshops, one in April 2008 in Koenigswinter, Germany and the other in San Francisco (July 2008). The July, 2008, workshop was organized with the express objective of evaluating the relative maturity of the entire set of emerging logic technologies that had been tracked by the ITRS ERD since 2001. The conclusion of this workshop was that none of the ERD tracked technologies was likely to replace scaled CMOS as the dominant information processing technology, but that some technologies had the potential to be superior to scaled silicon in certain specialized applications. Among these technologies, carbon-based nanoelectronics was judged to be the most mature and as such could benefit most from additional research funding. It was also explicitly concluded that all of the technology entries should continue to receive additional funding because it would premature to eliminate any of the options completely. A similar assessment of emerging memory technologies, held in April 2010, concluded that spin transfer torque MRAM and a "Redox" resistive memory were good candidates for accelerated research and development – thus ERD's continuing focus on spin nanodevices.

Logistics: The workshop will be held on September 17, 2010, in Sevilles, Spain, in conjunction with the 2010 ESSDERC Conference. A registration fee of 150 Euros will be charged to all participants. Also, the travel expenses for academic presenters can be reimbursed up to $2000 based on a grant from NSF. A detailed agenda is given below.

8:00-8:15 AM Welcome and Introduction

8:15 AM – 12:15 Evaluate status, progress, and research needs for spin based logic elements[1]

Moderator: George Bourianoff

- Overview of DARPA Spin Logic program (Dev Shenoy, DARPA)
- Nano-magnetic Logic (Sharon Hu, Notre Dame Univ.)
- All spin logic (Behtash Behin-Aein, Purdue University)
- Magnetic FPGAs, memory in logic (Takahiro Hanyu, Tohoku University)
- "TIMARIS: Linear Dynamic Deposition technology for production of Spintronic Devices" (Wolfram Maass, Singulus)
- Wrap-up discussion (30 min)

12:15 -1:15 PM Lunch

1:15- 5:15 PM Evaluate status, progress, and research needs for graphene logic devices

Moderator: Jim Hutchby

- "Graphene logic devices" (Philip Kim, Columbia University)
- "RF and Analog Graphene based FETs" (C. Y. Sung, IBM)
- "GRAND perspectives of graphene electronics" (Heinrich Kurz, AMO)
- "Gate-induced band gap for graphene devices" (Kazuhito Tsukagoshi, NIMS)
- "Graphene Research at CEA" (Stephan. Roche, CEA)
- Wrap-up discussion (30 min)

5:15-5:30 PM Break

5:30-6:30 PM Business meeting

General information: Presentation at the workshop is by invitation only. Attendance at the workshop is open to all interested parties who wish to participate.

Logistics: The workshop will be held on September 17 in Seville, Spain in conjunction with the 2010 ESSDERC Conference. A registration fee of **$200 USD** will be charged to all participants.

[1] Spin based logic elements mean complex gates defined by electrical inputs and outputs where all internal information processing is done by manipulating magnetic materials, fields and polarizations (e.g. 1 bit magnetic full adder) without internal electron transport.